

Mechano-Informatics (Subject)

Date : H25(2013), August 19th, 14:00 – 16:00

Instruction:

- 0) Answers should be written either in Japanese or English.
- 1) Do not open this problem booklet until the start of the examination is announced.
- 2) Three problems are provided. Solve Problem 1 (Compulsory), and solve either Problem 2A or Problem 2B (Required Elective).
- 3) When you have multiple interpretations of a problem statement, you may clarify your interpretation by introducing adequate definitions and/or conditions in your answer.
- 4) If you find missing, misplaced, and/or unclearly printed pages in the problem booklet, notify the examiner.
- 5) Two answer sheets are provided. Check the number of them, and if you find excess or deficiency, notify the examiner. You must use a separate sheet for each problem. When you run short of space for your answer on the front side of the answer sheet, you may use the back side by clearly stating so in the front side.
- 6) In the designated blanks at the top of each answer sheet, write examination name “Mechano-Informatics (Subject)”, “Master” or “Doctor”, your applicant number, and the problem number. Failure to fill up these blanks may void your test score.
- 7) An answer sheet is regarded as invalid if you write marks and/or symbols unrelated to the answer.
- 8) Even if the answer sheet(s) is blank, submit all answer sheets with examination name, “Master” or “Doctor”, your applicant number, and the problem number.
- 9) Use the blank pages in the problem booklet for your draft.
- 10) Fill in the blank below with your applicant number, and submit this booklet. Also submit the Japanese booklet with your applicant number in the corresponding blank.

Applicant number:

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Problem 1 (Compulsory)

P. 1. Consider processing the 7×7 grayscale image shown in Fig.1 by making convolutions between the image and a 3×3 filter. Give an example of filters described in (1) and (2), respectively. After applying each filter to the image, answer the resultant values at positions of (2, 2) and (4, 4) in the image. Note that the sum of the absolute values of 9 elements of each filter must be 1.

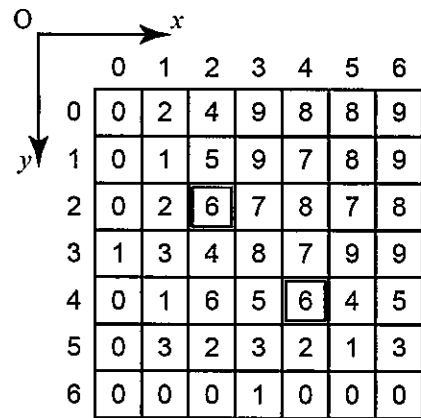


Fig.1

- (1) A smoothing filter
- (2) An edge filter along y -axis

P. 2. Describe the function of each resistor R shown in Fig.2 and Fig.3. Also derive each appropriate value of resistance. Here, the voltage of the digital input and output pins of the microcontroller in the figures is 5 V for HIGH or 0 V for LOW. In Fig.2, the leak current at the digital input pin is negligible and the consumed power of the resistor when the switch is pushed must be equal to or lower than 10 mW. In Fig.3, the maximum sink current at the digital output pin is 20 mA. The characteristic of the LED is shown in Fig.4.

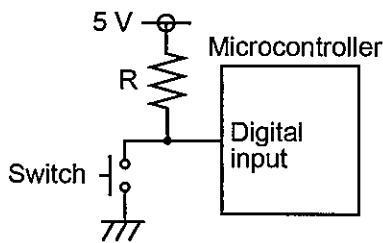


Fig.2

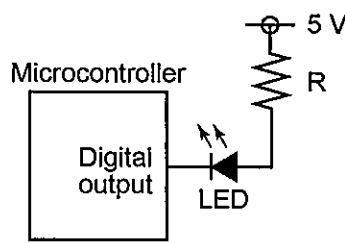


Fig.3

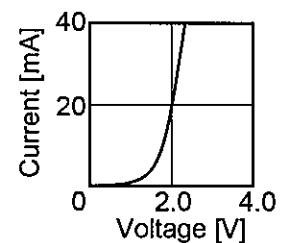


Fig.4

P. 3. Consider the two-link planar manipulator in Fig.5. The link lengths are l_1 and l_2 , and the joint angles are θ_1 and θ_2 . The coordinate of the tip is $\mathbf{p} = [x_p \ y_p]^T$.

- (1) Derive the velocity of the tip $\dot{\mathbf{p}} = [\dot{x}_p \ \dot{y}_p]^T$ when the links move with angular velocities of $\dot{\theta}_1$ and $\dot{\theta}_2$.
- (2) Derive the force generated at the tip $\mathbf{F} = [F_x \ F_y]^T$ when the manipulator is in static equilibrium and the torques τ_1 and τ_2 are applied to the joints of the manipulator as shown in Fig.6.

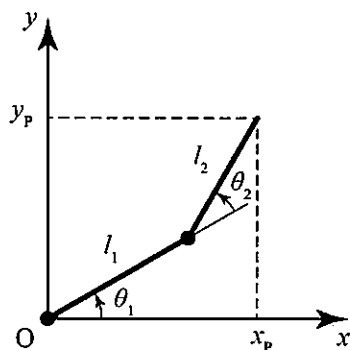


Fig.5

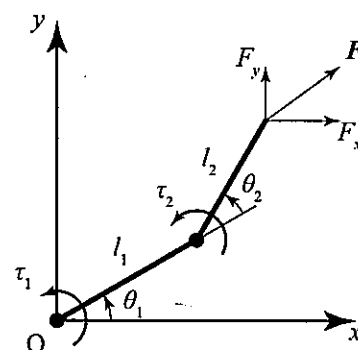


Fig.6

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Problem 2A (Required Elective)

Consider a system of Fig.1 consisting of a motor connected to a rigid body through a torsion spring. Viscous forces act on the rigid body and the motor. Let θ_1, θ_2 be rotational angles of the rigid body and the motor, J_1, J_2 be the moments of inertia with respect to the rotational axes, and c_1, c_2 be the viscous damping coefficients. Let k be the torsional spring constant and τ be the motor torque. The equations of motion of the rigid body and motor are as follows:

$$J_1 \ddot{\theta}_1 + c_1 \dot{\theta}_1 - k(\theta_2 - \theta_1) = 0$$

$$J_2 \ddot{\theta}_2 + c_2 \dot{\theta}_2 + k(\theta_2 - \theta_1) = \tau$$

Given $J_1 = 2, J_2 = 1, c_1 = 2, c_2 = 1, k = 2$, answer the following questions.

- P. 1. Define a state vector as $x = [\theta_1 \ \theta_2 \ \dot{\theta}_1 \ \dot{\theta}_2]^T$, and an input as $u = \tau$. The state equation is given by $\dot{x} = Ax + bu$. Find **A** and **b**.
- P. 2. Determine if this system is controllable.
- P. 3. Define an output as $y = \theta_1 - \theta_2$. The output equation is given by $y = Cx$. Find **C** and verify that this system is not observable.
- P. 4. In order to make this system observable, we choose $y = [\theta_1 \ \theta_2]^T$ as an output vector. We design an observer as $\dot{z} = Az + bu + K(y - Cz)$ with a state estimate z . Assuming that the observer gain **K** is given as follows, derive a condition with $k_{11}, k_{12}, k_{21}, k_{22}$ for the state estimate z to converge to the actual state x .

$$K = \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \\ -1 & 1 \\ 2 & -2 \end{bmatrix}$$

- P. 5. We design a state feedback system with an input $u = Fz$, where z is the state estimate derived in P.4. The whole system can be expressed as

$$\begin{bmatrix} \dot{x} \\ \dot{e} \end{bmatrix} = \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} \begin{bmatrix} x \\ e \end{bmatrix},$$

where $e = x - z$. Derive $P_{11}, P_{12}, P_{21}, P_{22}$ with **A, b, C, K, F**. In addition, verify that the poles of the whole system consist of the poles of the observer and the poles of the state feedback.

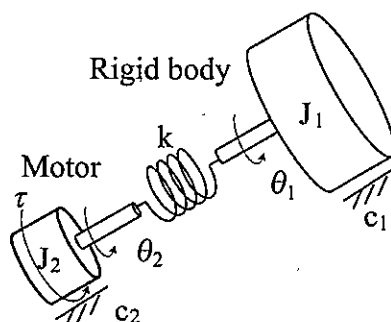


Fig.1

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Problem 2B (Required Elective)

Answer the following questions concerning on adders. Here, only two-input AND gates, two-input OR gates and NOT gates can be used as logic gates. Use MIL symbols for drawing schematic diagrams (see Fig.1). Assume that each variable in the following questions depicts a binary digit. For variables A and B , logical conjunction, logical disjunction and negation are expressed with $A \cdot B$, $A + B$ and \bar{A} , respectively.

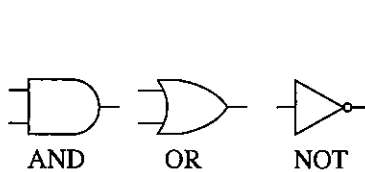


Fig.1

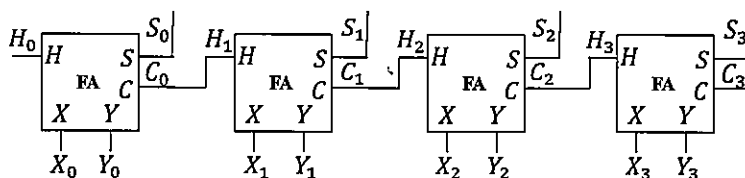


Fig.2

- P. 1. A one-bit full adder is denoted by FA. Let X and Y be the operands to the adder, and H be the carry-in from the lower bit as the input of FA. Let S be the sum, and C be the carry-out as the output of FA. Show the truth table of FA.
- P. 2. Assuming that the gate delay of each logic gate is T_0 , draw a schematic diagram of FA so as to make the propagation delay T_F of FA as short as possible. Obtain T_F using T_0 .

Consider structure of adders for four-bit digits $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$. Let H_j , X_j and Y_j be the inputs, and S_j and C_j be the outputs of FA for j -th bit operation ($j = 0, \dots, 3$). For each bit, logical conjunction and disjunction are expressed with $G_j = X_j \cdot Y_j$, $P_j = X_j + Y_j$, respectively.

- P. 3. A four-bit adder constructed by cascading four FAs as shown in Fig.2 is denoted by Adder-I. Obtain the propagation delay T_I of Adder-I using T_0 .
- P. 4. Express H_3 with G_0 , G_1 , G_2 , P_1 and P_2 . If necessary, use $C_j = G_j + H_j \cdot P_j$.
- P. 5. Let us build a circuit M that has G_0 , G_1 , G_2 , P_1 and P_2 as the inputs, and H_1 , H_2 and H_3 as the outputs. Draw a schematic diagram of the circuit M so as to minimize the propagation delay T_M of the circuit M, and obtain T_M using T_0 .
- P. 6. A four-bit adder using the circuit M and four FAs is denoted by Adder-II. Obtain the minimum propagation delay T_{II} of Adder-II using T_0 .
- P. 7. Describe advantage(s) and disadvantage(s) of Adder-II compared with Adder-I, when the number of bits of the adder operands is increased.

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