Master Course Entrance Examination Problem Booklet

Information Physics and Computing

Tuesday, August 22, 2017 10:00~13:00

Answer three out of Problems 1-5.

Note:

(1) Do not open this booklet until the starting signal is given.

(2) You should notify the examiner if there are missing or incorrect pages in your booklet. No questions relating to the contents of the problems are acceptable in principle.

(3) Three answer sheets will be given. Use one sheet per a problem. You may use the back of the sheet if necessary.

(4) Do not forget to fill the examinee's number and the problem number in the designated place at the top of each answer sheet. Do never put your name.

(5) Do not separate the draft papers from this booklet.

(6) Any answer sheet with marks or symbols unrelated to the answer will be invalid.

(7) In the case that a problem can be interpreted in several ways, you may answer the problem adding suitable definitions or conditions.

(8) Do not take the answer sheets and this booklet out of the examination room.

Examinee's number	

Fill this box with your examinee's number.

Problem numbers you selected			

Fill these boxes with the problem numbers you selected.

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Problem 1

Answer the following questions regarding Fourier series and digital filter design. Note that the digital signal to be filtered is digitized with an appropriate anti-aliasing filter.

(1) Calculate Fourier coefficient $f_1[n]$ of periodic pulse $F_1(\omega)$ as shown in Fig. 1 (width: A $(0 < A < 2\pi)$, height: 1, and period: 2π). Note that the Fourier coefficient is expressed as

$$f_1[n] = \frac{1}{2\pi}\int_{-\pi}^{\pi} F_1(\omega)\exp(\mathrm{j}\omega n)\mathrm{d}\omega,$$

where j is the imaginary unit. Now, $F_2(\omega)$ is the function generated by shifting $F_1(\omega)$ by π on the ω axis as shown in Fig. 2. Calculate Fourier coefficient $f_2[n]$ of $F_2(\omega)$.

(2) In the case that Fourier series $f_3[n]$ is a real-valued and even function, explain whether $F_3(\omega)$ whose Fourier series is $f_3[n]$ is a real-valued or purely imaginary-valued function and whether $F_3(\omega)$ is an even or odd function. If $f_3[n]$ is a real-valued and odd function, answer the same questions about $F_3(\omega)$.

(3) Under the situation in Question (1), let us consider that ω is the normalized angular frequency, n is the discrete time, and $F_1(\omega)$ and $F_2(\omega)$ are ideal frequency responses of digital filters (denoted by $F_1(\exp(\mathrm{j}\omega))$ and $F_2(\exp(\mathrm{j}\omega))$, hereafter).

(a) What type of frequency-selective filters are $F_1(\exp(\mathrm{j}\omega))$ and $F_2(\exp(\mathrm{j}\omega))$?

(b) Let $\{b_{1,n}\}$ $(n=0, 1,\ldots, 2M)$ be the FIR filter corresponding to $f_1[n]$ that is calculated in Question (1). $\{b_{1,n}\}$ is generated by the following procedure: (i) extracting the values of $f_1[n]$ in a duration of $-M \le n \le M$ $(M > 0)$ and then (ii) time-shifting them by M points. From the viewpoint of FIR filter design, explain this extraction and time-shift procedure with technical terms of signal processing.

(4) Let us consider a digital filter whose impulse response $f_4[n]$ is 0 for a duration of $n < -4$, $4 < n$ and real otherwise. As shown in Fig. 3, the frequency response of $f_4[n]$, $F_4(\exp(\mathrm{j}\omega))$, is a real-valued and even function. FIR filter $\{b_{4,n}\}$ $(n=0,1,\ldots, 8)$ is generated by the extraction and time-shift procedure described in Question (3)-(b) for $f_4[n]$ $(M=4)$.

(a) Find phase response $\arg\{B_4(\exp(\mathrm{j}\omega))\}$ of FIR filter $\{b_{4,n}\}$ and draw a general shape of $\arg\{B_4(\exp(\mathrm{j}\omega))\}$ for a duration of $-\pi \le \omega \le \pi$.

(b) Figure 4 shows FIR filter $\{b_{4,n}\}$ only for a duration of n=0,1,..., 4. Draw the remaining part and complete the whole outline. Also, explain the reason for doing so.

(5) Frequency response $F_5(\exp(j\omega))$ (solid line) is generated by superposing $jF_4(\exp(j(\omega-\psi)))$ (dashed line) and $jF_4(\exp(j(\omega+\psi)))$ (dotted line) ($0 < \psi < \pi/2$) as shown in Fig. 5, where $F_4(\exp(j(\omega)))$ is described in Question (4).

(a) Express impulse response $f_5[n]$ corresponding to $F_5(\exp(j\omega))$ by using $f_4[n]$.

(b) FIR filter $\{b_{5,n}\}$ is generated by the extraction and time-shift procedure described in Question (3)-(b) for $f_5[n]$. Discuss the zeros that FIR filter $\{b_{5,n}\}$ always has.

(c) What type of frequency-selective filter is FIR filter $\{b_{5,n}\}$? Also, discuss usage of it.

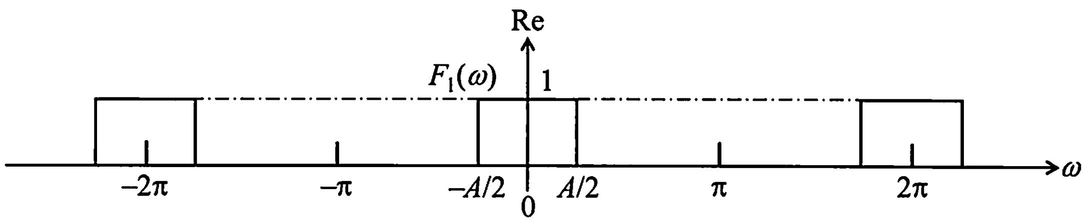

Fig. 1

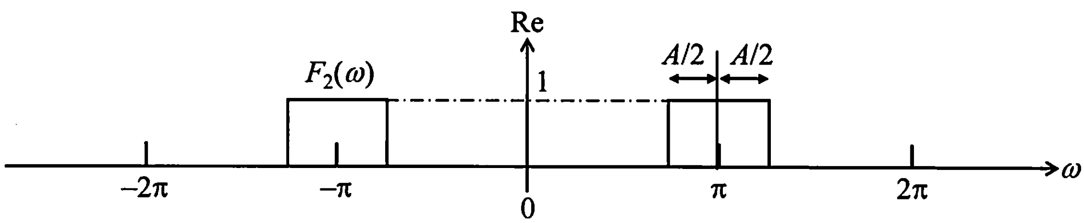

Fig. 2

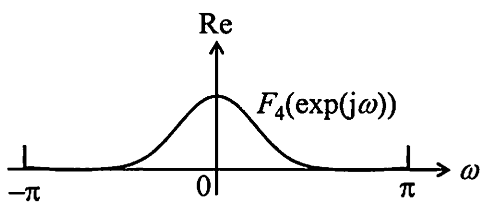

Fig. 3

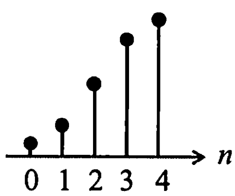

Fig. 4

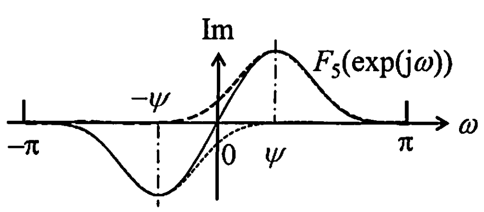

Fig. 5

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Problem 2

Answer the following questions about the electric circuits by using operational amplifiers. Assume that all the operational amplifiers in this problem have ideal characteristics.

(1) Derive the differential equation that represents the relationship between input voltage $v_1(t)$ and output voltage $v_2(t)$ of the electric circuit shown in Fig. 1, and obtain transfer function $G(s)$ from $v_1(t)$ to $v_2(t)$.

(2) Draw the gain characteristics of $G(s)$ obtained in Question (1), $|G(\mathrm{j}\omega)|$, by the straight-line approximation. For this drawing, the scales of the horizontal axis is $\log_{10}\omega$, and the vertical axis is dB expressed by $20\log_{10}|G(\mathrm{j}\omega)|$. In particular, specify the break angular frequencies, the slopes, and the gains at the break points.

(3) Derive the differential equation that represents the relationship between input voltage $v_1(t)$ and output voltage $v_2(t)$ of the electric circuit shown in Fig. 2. Next, obtain $v_2(t)$ when $v_1(t)$ is a step input with amplitude a rising up at t=0, and show the conditions under which $v_2(t)$ is not divergent. Assume that voltage across capacitor C is 0 at t=0.

(4) Describe the behaviors of the electric circuit shown in Fig. 3 according to the following questions.
   (a) Derive the differential equation that voltage $v(t)$ in the electric circuit satisfies.
   (b) Now $v(t)$ is sustainably oscillating. Show the conditions for sustained oscillation of $v(t)$ and the oscillation frequency by using resistances R_1, R_3, R_4, and r, variable resistance R_2, and capacitance C used in the circuit.
   (c) In Question (4)-(b), explain how $v(t)$ changes when variable resistance R_2 is increased or decreased slowly. Assume the power supply voltage of the operational amplifiers is infinite.

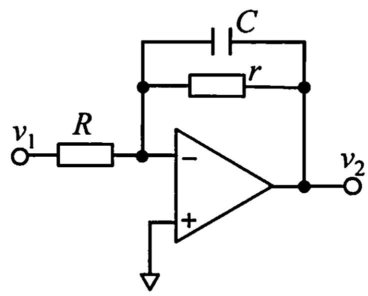

Fig. 1

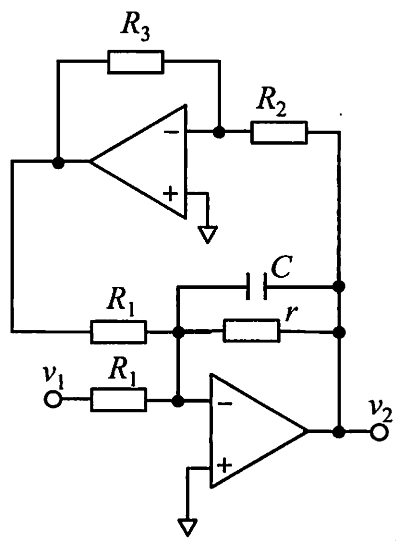

Fig. 2

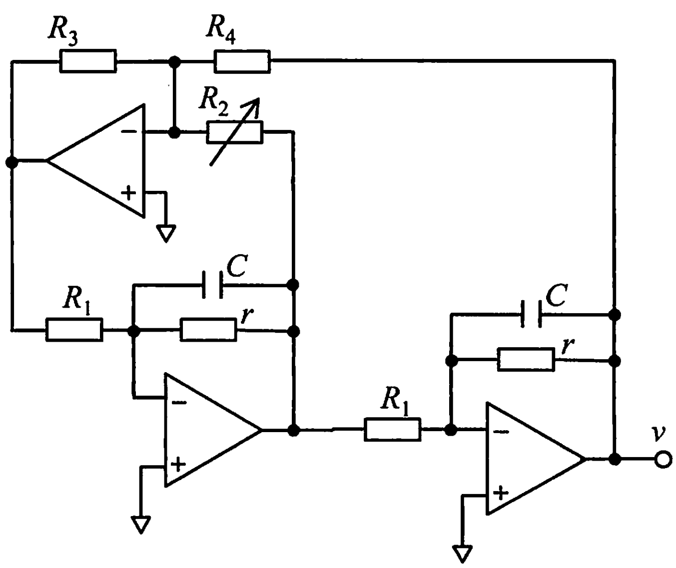

Fig. 3

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Problem 3

(1) Let us consider a closed loop system shown in Fig. 1, where $P(s) = \dfrac{s+1}{s^2 - s + 1}$ and K is a constant gain. Show the condition on K such that the closed loop system is stable.

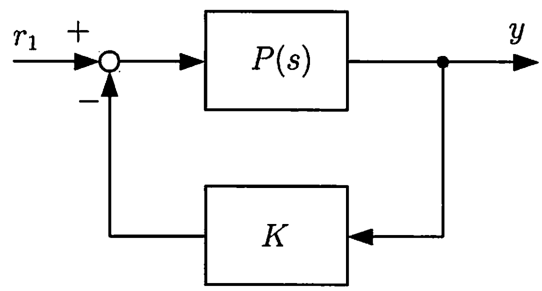

Fig. 1

(2) In Question (1), let us denote the transfer function from r_1 to y by $G_1(s)$ where K is given such that $G_1(s)$ is stable.

(a) Show the condition on K such that the following condition is satisfied:

$$\mathrm{Re}\left[G_1(\mathrm{j}\omega)\right] > 0, \text{ for } |\omega| < \infty$$

(b) Show the Nyquist diagram of $G_1(s)$ in the case of Question (2)–(a). If the diagram has points crossing and/or touching the real axis, show the formulas of the points.

(3) As shown in Fig. 2, let us connect $C_1(s)$ with $G_1(s)$ given in Question (2)–(a), where $C_1(s)$ is stable and satisfies

$$\mathrm{Re}\left[C_1(\mathrm{j}\omega)\right] > 0, \text{ for } |\omega| < \infty.$$

Explain the stability of the closed loop system by using the Nyquist stability criterion.

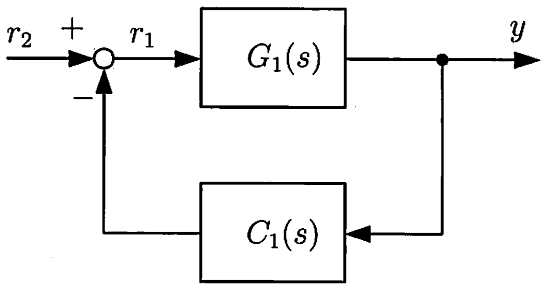

Fig. 2

(4) As shown in Fig. 3, let us connect $C_i(s)$, $i = 1, 2, \ldots, N$, with $G_1(s)$ given in Question (2)–(a), where $C_i(s)$ are stable and satisfy

$$\mathrm{Re}\left[C_i(\mathrm{j}\omega)\right] > 0, \text{ for } |\omega| < \infty, \forall i.$$

Explain the stability of the closed loop system by using the Nyquist stability criterion.

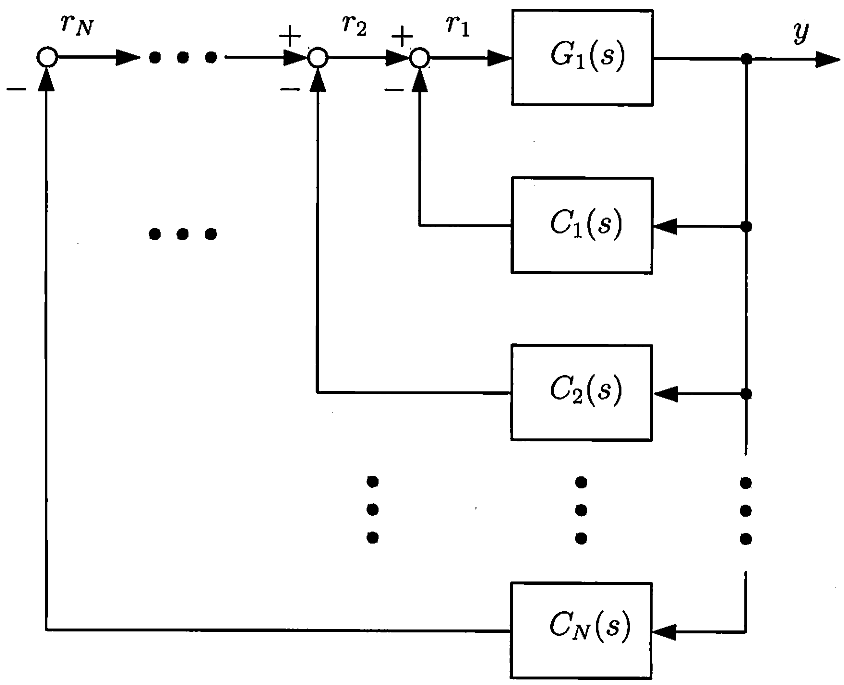

Fig. 3

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Problem 4

Answer the following questions on logic circuits.

(1) Consider an electrical lock which is open when three consecutive 2-bit binary numbers in an input sequence are matched to specific consecutive numbers. Suppose that the electrical lock is implemented by using the logic circuit shown in Fig. 1. In the figure, f_M indicates a control circuit block. DFF_1 and DFF_2 indicate D flip-flops which hold state variables. Let (x_1,x_2), *unlock*, and *clk* denote 2-bit input variables, a 1-bit output variable, and a clock signal to the D flip-flops, respectively. The output variable *unlock* indicates that the electrical lock is open when the value is 0 and closed when the value is 1. Let (y_1,y_2) and (z_1,z_2) denote 2-bit input and output signals to and from the D flip-flops, respectively. Here, assume that the electrical lock is open when a sequence of input values of (x_1,x_2) is (1,1),(0,1),(1,0). After the electrical lock is open, it is closed when the next value is input and accepts another input sequence again. Suppose that a 2-bit binary number (x_1,x_2) is input every clock cycle.

(a) Illustrate a state transition diagram for implementing the electrical lock by a Mealy state machine using at most four states denoted as q_0, q_1, q_2, and q_3.

(b) Show the truth table for *unlock* and (y_1,y_2) output from the control circuit block f_M. Assume that the correspondence between states from q_0 to q_3 and the state variables stored in DFF_1 and DFF_2 follows Table 1.

(c) Give a minimum sum-of-products expression of (y_1,y_2).

(2) Next, consider to implement the electrical lock described in Question (1) by a Moore state machine.

(a) Illustrate a state transition diagram.

(b) Explain advantages and disadvantages of a Mealy state machine compared with a Moore state machine.

(3) Consider the following Eq. (1) for an n-variable logic function $f(x_1,\cdots,x_i,\cdots,x_n)$.

$$f(x_1,\cdots,x_i,\cdots,x_n) = \overline{x_i}\cdot f(x_1,\cdots,0,\cdots,x_n) + x_i \cdot f(x_1,\cdots,1,\cdots,x_n) \quad (1)$$

(a) Prove that Eq. (1) holds.

(b) For an arbitrary four variable logic function $f(x_1, x_2, x_3, x_4)$, derive the Boolean expression in a sum-of-products form consisting of only minterms and constants, using Eq. (1).

(c) Explain that Boolean expressions of output variables of control circuit block f_M in Question (1) can be derived using Eq. (1).

(4) Let us re-design the electrical lock considered in Question (1) in order that it is open when the three 2-bit input values (1,1),(0,1),(1,0) are input consecutively in an arbitrary order without repetition as the input of (x_1,x_2). For example, if an input sequence is (0,0),(0,1),(1,0),(0,1),(1,1), the electrical lock is open when the last value (1,1) is input. Illustrate the circuit diagram to implement this electrical lock using two shift registers consisting of DFFs shown in Fig. 2. In the circuit diagram, besides the shift registers, you may use 2-bit equality comparators shown in Fig. 3, AND gates, OR gates, and NOT gates.

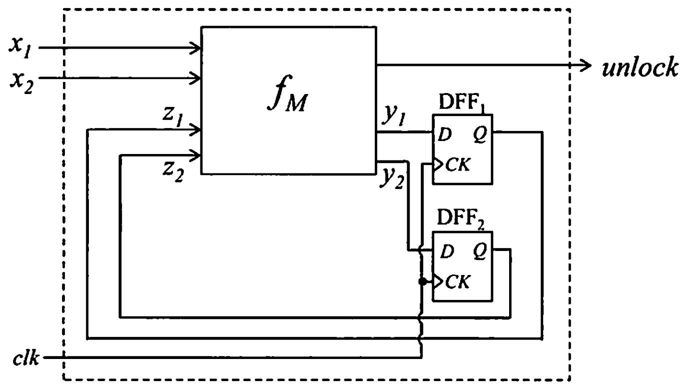

Fig. 1

Table 1

State	DFF$_1$	DFF$_2$
q_0	0	0
q_1	0	1
q_2	1	0
q_3	1	1

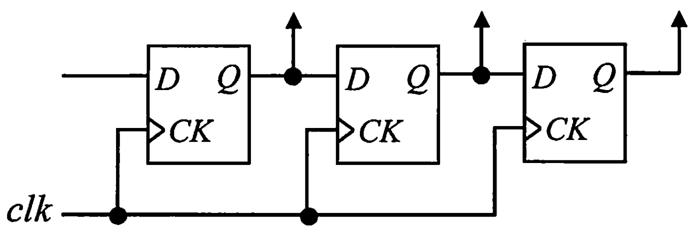

Fig. 2

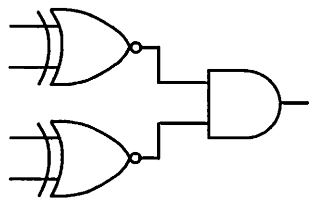

Fig. 3

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Problem 5

Consider a cylinder C of mass M, outer radius a, inner radius b, and height h as shown in Fig. 1. Assume that the density of C is homogeneous. Denote the gravitational acceleration by g. Answer the following questions.

(1) Find the moment of inertia I of C about its central axis.

(2) Suppose that C rolls down a plane inclined at an angle of α, starting from rest, as shown in Fig. 2. The central axis of C is parallel to the x-axis. The coefficient of static friction between C and the plane is μ. Find the condition for α and μ such that C rolls without slipping.

(3) In Question (2), find the velocity w of the centroid of C when it moves by distance L along the inclined plane from a position of rest. Also, answer whether w increases or decreases when b is increased while M, a, and h are fixed, and explain the reason from the viewpoint of law of conservation of energy.

(4) As shown in Fig. 3, C is put on a flat plate moving with a constant velocity of u_0. Discuss the motion of C. Define constants, variables, and conditions if necessary.

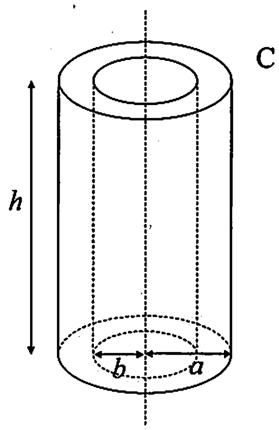

Fig. 1

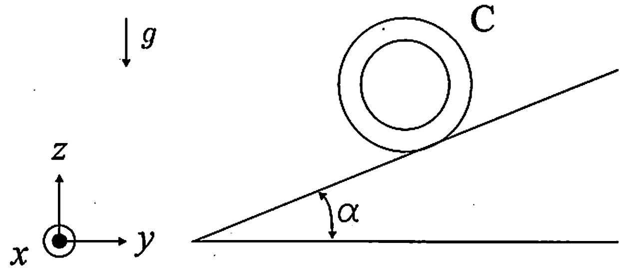

Fig. 2

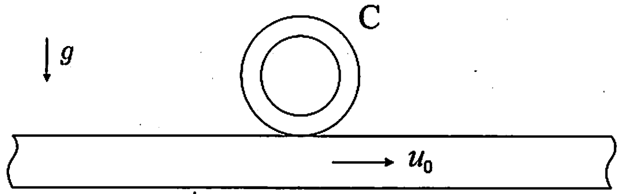

Fig. 3

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