Specialized Subjects

9:00～11:30, Wednesday, August 22, 2007

Instructions

1. Do not open this booklet before permission is given.

2. This booklet contains 6 problems. The number of pages is seven excluding this cover sheet and blank pages. If you find missing or badly printed pages, ask the attendant for exchange.

3. Answer three problems. You can select any three out of the six. Your answer to each problem should be written on a separate sheet. You may use the reverse side of the sheet if necessary.

4. Fill the top parts of all your three answer sheets as instructed below. Before submitting your answer sheets, make sure that the top parts are correctly filled.

専門科目

第一問

↑
Write the Problem No.

↑
Write the Examinee No.

5. The three answer sheets must be submitted at the end of the examination, even if they are blank ones.

6. You must answer either in Japanese or in English.

7. This booklet and the preparation sheet must be returned at the end of the examination.

8. This English translation is informal but provided for the convenience of applicants. Japanese version is the formal one.
blank page
Problem 1

The circuit in Fig. 1 is composed of resistors and a capacitor, and the switches $S_1$ and $S_2$ are open. At time $t = 0$, the switch $S_1$ is closed and the constant voltage $E_0$ is applied to the circuit.

1. Obtain the impedance $Z(s)$ of the circuit when $S_1$ is closed and $S_2$ is open.
2. Derive the current $I(s)$ and the voltage $V_{\text{out}}(s)$ between the capacitor terminals in Fig. 1. Here, $I(s)$ and $V_{\text{out}}(s)$ are the Laplace transforms of the current and the voltage, respectively.
3. Derive the transient response of the output voltage $V_{\text{out}}(t)$ through the inverse Laplace transform of $V_{\text{out}}(s)$.
4. Suppose the switch $S_2$ be closed just when $V_{\text{out}}(t) = E_1$ at time $t = t_1$ in the circuit of Fig. 1. Obtain the time constant $\tau$ of the circuit and the output voltage $V_{\text{out}}(t)$.

The rightmost element in Fig. 2 is a neon lamp. The neon lamp will be on and start discharging when the voltage between its terminals are higher than $E_1$, and will stop discharging when the voltage goes down lower than $E_2$. You can regard the neon lamp as a resistance $r$ when discharging.

5. Obtain the condition such that the neon lamp turns on and off repeatedly. Then draw a graph of the voltage $V_{\text{out}}$ versus $t$.
6. Obtain the on-off interval of the neon lamp.

![Fig. 1](image1)

![Fig. 2](image2)
Problem 2

Answer the following questions about a processor with the instruction pipeline. The pipeline is composed of the following five stages: instruction fetch (F), instruction decode and register read (D), execution (E), memory access (M) and write-back (W). Each of the stages takes one cycle.

(1) Explain three fundamental types of pipeline hazard: structural, control, and data hazards.

(2) Fig. 1 shows assembly code for the processor. In the figure, I1, ..., I6 indicate the labels, r1, ..., r4 indicate the registers. The notation \([r1 + o]\) \((o = 0, 4)\) in the load/store instructions I1 (I2, I6) indicates that the memory access is performed to the address calculated by adding \(o\) to the contents of \(r1\). The conditional branch instruction “be” labeled I4 transfers the control to the instruction I6 depending on the contents of the register r4.

Show the pipeline diagram that represents how the instructions of the code flow through the instruction pipeline when the branch instruction I4 is not-taken, using Fig. 2 as reference. And then calculate the CPI (Cycles Per Instruction), and indicate all the positions where the control and data hazards appear in the diagram.

The processor has the following restrictions: the memory accesses in the I and M stages cannot be executed in parallel; the result of each instruction is once written back into the register file, and then read by other instructions; on the execution of branch instructions, the branch direction is decided in the D stage, the branch target address is calculated in the E stage and set to the PC (program counter) in the W stage, respectively.

\[
\begin{align*}
\text{I1:} & \quad \text{load} & r2 &= [r1 + 0]; & \text{I1:} & \quad F&D&E&M&W \\
\text{I2:} & \quad \text{load} & r3 &= [r1 + 4]; & \text{I2:} & \quad F & \ldots \\
\text{I3:} & \quad \text{sub} & r4 &= r2 - r3; & \text{I3:} & \quad \\
\text{I4:} & \quad \text{be} & r4, I6; & \text{I4:} & \quad \\
\text{I5:} & \quad \text{sub} & r4 &= 0 - r4; & \text{I5:} & \quad \\
\text{I6:} & \quad \text{store} & [r1 + 0] &= r4; & \text{I6:} & \quad 
\end{align*}
\]

Fig. 1

Fig. 2

(3) The extra cycles caused by structural, control and data hazards can be reduced by relaxing the restrictions specified in (2). Answer such architectural techniques for structural, control, and data hazards, respectively.

Show the pipeline diagram when all the techniques are adopted, and then calculate the CPI.
Problem 3

You have collected 1 billion web pages from WWW, and are going to store and organize them. You should make various indices of these pages and their attributes to enable search by a given URL. However, URLs are inconvenient to use as keys for the indices, because the lengths of URLs vary from tens of bytes to over one thousand bytes (about 50 Bytes on average). Therefore, you first need to assign IDs (sequentially ordered integers from 1 to \( N \)) to URLs, and build indices that map from IDs to URLs and back again.

1. Describe a data structure that stores a mapping from IDs to URLs, and allows search for a URL from a given ID in \( O(1) \) time. You should minimize the memory space without compression.

2. Estimate the required memory space for storing 1 billion URLs in the data structure you described in (1).

3. Describe a data structure that stores a mapping from URLs to IDs, and allows search for an ID from a given URL in \( O(1) \) time on average. You should minimize the memory space without compression.

4. Estimate the required memory space for storing 1 billion URLs in the data structure you described in (3).
Problem 4

(1) Show the Nyquist frequency (the minimum sampling frequency) $f_{Ny}$ [Hz] and the Nyquist interval $T_N$ [sec] for a signal $g(t)$ whose spectrum is band-limited to $B$ [Hz].

(2) Derive and draw the impulse response $h(t)$ of $H(\omega) = T_s \text{rect}\left(\frac{\omega}{4\pi B}\right)$ shown in Fig.1, where $H(\omega)$ is the ideal interpolating filter function of bandwidth $B$ [Hz], and $T_s$ [sec] is the sampling interval corresponding to the sampling frequency $f_s$ [Hz].

(3) Let $\sum_{l=-\infty}^{\infty} g(lT_s)\delta(t-lT_s)$ be the sampled signal by sampling at $f_s \geq f_N$ [Hz] a signal $g(t)$ whose spectrum is band-limited to $B$ [Hz], where $\delta(t)$ is the unit impulse function or the delta function. Explain $g(t) = \sum_{l=-\infty}^{\infty} g(lT_s)h(t-lT_s)$.

(4) For any integer $n$, show $g(nT_s) - g(nT_s)h(0) = \sum_{l=n}^{\infty} g(lT_s)h((n-l)T_s)$ and $g(nT_s) - g(nT_s)h(0) = g(nT_s)(1-2BT_s)$.

(5) The time division multiplexing system for $M$ analogue data channels shown in Fig.2 has $M$ independent input channels $C_m$ and output channels $O_m$ $(0 \leq m \leq M-1)$. Let the values of $C_m$ and $O_m$ at time $t$ be $c_m(t)$ and $o_m(t)$ respectively, where all the $c_m(t)$ s change their values simultaneously once a second, as shown in Fig.3. Hence $c_m(t) = c_m(i)$ $(0 \leq m \leq M-1)$ at $t_{i,m} = i + m/M$ [sec], and puts it as $c_m(i)\delta(t-t_{i,m})$ into the ideal interpolation filter $H(\omega)$ of bandwidth $B$ [Hz], shown in Fig. 1. Then $x_D(t) = \sum_{i=-\infty}^{\infty} \sum_{m=0}^{M-1} c_m(i)\delta(t-i - \frac{m}{M})$ is a sampled signal of the sampling interval $T_s = \frac{1}{M}$. $x_D(t)$ is sent over $H(\omega)$ and $x(t)$ is received at the receiver side $S_O$. At $S_O$ synchronized to $S_I$, $x(t)$ is sampled at $t_{i,m}$ [sec], held by the circuit $SH_m$ for 1 second, and finally sent out to the output channel $O_m$. Explain $o_m(t) = c_m(t - m/M)$ as in Fig.4, and find the number of channels $M$ to transmit $M$ independent signals $c_m(t)$. 
Problem 5

Assume a single server communication system where the packets arrive with the average arrival rate of $\lambda$ [1/sec] and where the mean service time of these packets is $1/\mu$ [sec]. After being served, each packet departs the system. When the server is occupied, arrived packets are stored at a buffer and served afterwards on a First-In, First-Out basis. We also assume that the length of the buffer is $L$, meaning that up to $L$ packets can wait there at the same time. The packets that arrive when there already exist $L$ waiting packets are lost.

First, in the following sub problems (1), (2) and (3), assume that the length of the buffer is infinite.

(1) Describe the condition where the system is not saturated in terms of the offered traffic $\alpha = \lambda / \mu$ [erl]. In all the followings, we assume that this condition holds and that there exists a steady state.

(2) Let $N$ and $W$ be the average number of packets and the average waiting time, respectively. Show Little’s formula, which describes the relation between $N$, $W$ and $\lambda$ in steady state. Also, describe the reason why this formula holds briefly.

(3) Assume that the packets arrive in a Poisson manner and that the service time is an exponential distribution. Let $p_k$ be the steady state probability where there are $k$ packets in the system. Show $p_k$ in terms of $\alpha$. Also show $N$ and $W$ in terms of $\alpha$ and $\lambda$.

Next, in the following sub problems (4), (5), (6) and (7), assume that the length of the buffer is finite.

(4) As in (3), assume that the packets arrive in a Poisson manner and that the service time is an exponential distribution. Show the packet loss probability in terms of $\alpha$ and $L$.

(5) The average loss rate depends on the traffic pattern even if the offered traffic is the same. Show a traffic pattern where the packet loss rate is larger than the case in (4) and explain it briefly. Then, compare the packet loss rate and the steady state probability with which there exist(s) $L$ packets under this traffic pattern. Answer which is larger and discuss it briefly.

(6) This time, show a traffic pattern where no packet loss occurs and explain it briefly.

(7) When the traffic is the same, the larger packet loss rate is not desirable. In order to avoid this circumstance, traffic pattern may be converted to another. Discuss the advantages and the disadvantages of implementing this method briefly.
Problem 6

A memory-less source outputs four symbols $x_1$, $x_2$, $x_3$ and $x_4$ with probabilities of 1/8, 1/8, 1/4 and 1/2 respectively. Answer the following questions.

(1) Design Huffman code for the four symbols. Discuss how much improvement of the efficiency of compression can be further obtained.

(2) Suppose two robots A and B are trained so that they respond to the four symbols and take actions $y_1$, $y_2$, $y_3$ and $y_4$. However, their recognition of the symbols is not perfect. According to the statistics, their performance is shown by conditional probabilities in the tables below. Obtain the probability that each robot correctly acts.

(3) Comparing robots A and B, which robot receives more amount of information from the source? Obtain the amount of information that each robot receives. Explain intuitively the reason that the one robot receives more than the other.

(4) Either robot A or B is modified so that amount of information received from the source is increased and the performance is reversed. Suppose the modification results in one exchange of two values in the conditional probability table. Show an example of such modification.

(Use $\log_2 3 = 1.58$, $\log_2 5 = 2.32$ if necessary.)

| Robot A | $P(y|x)$ | $y_1$ | $y_2$ | $y_3$ | $y_4$ |
|---------|----------|-------|-------|-------|-------|
| $x_1$   | 1        | 0     | 0     | 0     | 0     |
| $x_2$   | 0        | 1     | 0     | 0     | 0     |
| $x_3$   | 0        | 0     | 1     | 0     | 0     |
| $x_4$   | 0        | 1/4   | 1/4   | 1/2   |       |

| Robot B | $P(y|x)$ | $y_1$ | $y_2$ | $y_3$ | $y_4$ |
|---------|----------|-------|-------|-------|-------|
| $x_1$   | 1/2      | 1/2   | 0     | 0     |       |
| $x_2$   | 0        | 1/2   | 1/2   | 0     |       |
| $x_3$   | 0        | 0     | 1/2   | 1/2   |       |
| $x_4$   | 0        | 0     | 0     | 1     |       |